INSTRUCTION MANUAL

BIT 488/500

DIGITAL PROGRAMMING CARD

BIT 488-B, BIT 488-D, BIT 500-B, BIT 500-D

KEPCO INC. An ISO 9001 Company.	MODEL BIT 488/500 DIGITAL PROGRAMMING CARD
	ORDER NO. REV. NO

NOTE This on-line version of the Technical Manual includes only installation and operating instructions. For the complete manual, please contact Kepco.

©1999, KEPCO, INC.



TABLE OF CONTENTS

PARA	GRAPH	PAGE
	SECTION I—INTRODUCTION	
1-1	Scope of Manual	1-1
1-3	General Description	1-1
1-8	Specifications	1-2
1-11	Data Form	1-3
1-12	Accessories (Supplied)	1-3
1-13	Accessories (Optional)	1-3
	SECTION II—INSTALLATION	
2-1	Unpacking and Inspection	2-1/2-2
2-3	Installation of BIT card into the BOP	2-1/2-2
	SECTION III—OPERATION	
3-1	General	3-1
3-5	Digital Input Description, BIT-500B and BIT-500D Programming Cards	3-1
3-6	Digital Input Description, BIT-488B and BIT-488D Programming Cards	3-3
2.14	Coding Examples	o-o
2.10	GPIR Programming Notes for the experienced user	3-10
3-20	Calibration	3-11
	SECTION IV—THEORY OF OPERATION	
4-1	General	4-1
4-3	Digital Front-End RIT 488	
4 1 4	Analog Output Circuit	4-3/4-4
4-17	Digital Front-End, BIT 500	4-3/4-4
	SECTION V—PARTS LIST AND DIAGRAMS	
5-1	General	5-1/5-2
5-1 5-3	Ordering Information	5-1/5-2

LIST OF ILLUSTRATIONS

FIGU	RE	PAGE
1-1	Mechanical Outline Drawing	1-4
2-1	Installation of BIT-Card into BOP Power Supply	2-1/2-2
3-1	Digital Input Connector (PC-12) Wiring, BIT 500 Series	3-1
3-2	Timing Diagram, BIT 500 Series	3-3
3-3	Location of Address Selector Switch (BIT 488)	3-3
3-4	Location of Test Points and Calibration Controls on the (Installed) BIT-Card	3-11
3-5	Test Set-Up for BOP-BIT Calibration	3-12
3-6	Calibration Flow Chart, Part I	3-13
3-7	Calibration Flow Chart, Part II	3-14
4-1	Block Diagram, BIT 488 Programmer	4-5/4-6
4-2	Block Diagram, BIT 500 Programmer	
5-1	Component Location, BIT Programming Card	5-9/5-10
5-2	Schematic Diagram, BIT Programming Card	
		ţ
	LIST OF TABLES	
TABL	E	PAGE
1-1	Kepco BIT 488 and BIT 500 Digital Programming Cards	
1-1	Specifications, BIT 488 and BIT 500 Models	
1-2	opeonications, Bit 400 and Bit 600 modele	_
3-1	Listening Address Selection, BIT 488 Models	3-4
3-2	Control Character Coding, BIT 488 Models	
3-3	Coding Examples, BIT 500-D Models, Main Channel	
3-4	Coding Examples, BIT 500-D Models, Limit Channel	
3-5	Coding Examples, BIT 500-B Models, Main Channel	3-8
3-6	Coding Examples, BIT 500-B Models, Limit Channel	
4-1	BIT 488, Pin Assigments and Signal Line Sets	
4-2	Interface Message Repertoire, BOP/BIT 488	4-2

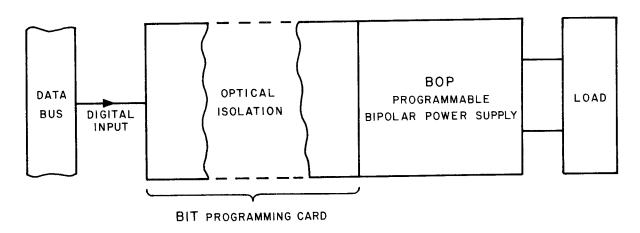
SECTION I—INTRODUCTION

1-1 SCOPE OF MANUAL

1-2 This manual contains instructions for the installation, operation and maintenance of the Series BIT DIGITAL PROGRAMMINGS CARDS manufactured by KEPCO, INC., FLUSHING, N.Y., U.S.A..

1-3 GENERAL DESCRIPTION

1-4 The Kepco BIT DIGITAL PROGRAMMING CARDS were designed as an accessory for the Kepco BOP series bipolar power supplies. The BIT cards made it possible to control the BOP output by means of digital input signals. The BIT card acts as an interface between the digital data bus and the BOP, accepting the digital input data and converting it to an analog signal which in turn, controls the BOP output.



1-5 The BIT design group consists of four models. Field installable programming cards carry the prefix "BIT". BOP bipolar power supplies with installed programming card carry the listed suffixes.

FIELD INSTALLABLE PROGRAMMING CARD MODEL	FACTORY INSTALLED PROGRAMMING CARD BOP SUFFIX	INPUT CODING	RESOL MAIN CHANNEL	REMARK		
B1T 488-B	488-B	BYTE-SERIAL	12 BITS (BINARY)	8 BITS (BINARY)	FOR THE IEEE-488	
BIT 488-D	488-D	BYTE-SERIAL	3-DIGIT (BCD)	2-DIGIT (BCD)	OR GPIB BUS	
BIT 500-B	500-B	BIT-PARALLEL	12 BITS (BINARY)	8 BITS (BINARY)	FOR PARALLEL DATA TRANSFER	
BIT 500-D	500-D	BIT-PARALLEL	3-DIGIT (BCD)	2-DIGIT BCD)	BUS	

TABLE 1-1 KEPCO BIT 488 and BIT 500 DIGITAL PROGRAMMING CARDS.

- 1-6 All BIT models, as listed in Table 1-1, have the following common features:
 - A) OPTICAL ISOLATION: Digital and analog grounds can be separated by a maximum of 500 volts.
 - B) TWO-CHANNEL OPERATION: Each channel can be independently programmed. The main channel (with higher resolution) may be dedicated for the control of either output voltage or output current, while the limit channel assumes the limit control of the complementary function.
 - C) POLARITY AND RANGE: The output range of the main channel is 0 to (±) 10V (high range) or 0 to (±) 1V (low range), selectable by digital input command. The output range of the limit channel is 0 to (+) 10V.

1-8 SPECIFICATIONS:

1-9 GENERAL SPECIFICATIONS: See Table 1-2.

	T						
OUTPUT VOLTAGE (MAIN CHANNEL)	HIGH RANGE: 0 ± 10V, LOW RANGE: 0 ± 1V						
OUTPUT VOLTAGE (LIMIT CHANNEL)	0 to +10V						
OUTPUT CURRENT (EACH CHANNEL)	0 to ±2 mA max.						
OUTPUT IMPEDANCE	< 0.05 ohms						
TEMPERATURE COEFFICIENT	FULL SCALE: \pm 35 PPM/ °C max. ZERO, HIGH RANGE: \pm 20 μ V/ °C max. ZERO, LOW RANGE: \pm 10 μ V/ °C max.						
LOGIC INPUT	TTL COMPATIBLE						
DIGITAL INPUT FORMAT	BYTE/SERIAL (BIT-488) BIT PARALLEL (BIT-500)						
INTERFACE FUNCTIONS IMPLEMENTED	AHI, LI, RL2, DC2 (BIT-488)						
POWER REQUIREMENT	SUPPLIED BY BOP						

TABLE 1-2 SPECIFICATIONS, BIT 488 AND BIT 500 MODELS.

1-10 TIMING:

1) Data Transfer Time.

BIT 500 Series: Approximately 50 microseconds. **NOTE**: Data must be present and stable during the STROBE pulse (2 microseconds minimum). Although the complete transfer requires 50 microseconds before the BIT 500 Programmer can be strobed again, the DATA BUS can be used for other instruments or programs following the end of the 2 microseconds STROBE pulse.

BIT 488 Series: Approximately 100 microseconds.

2) Data Transfer Rate: Determined by the data bus controller.

1-11 DATA FORM

BIT 500		BIT 488					
DATA FORM: BIT PARALLEL		DATA FORM: CMMMLL (BYTE SERIAL-BIT PARALLEL)					
MAIN CHANNEL FIELD	12 BITS	CONTROL CHARACTER (C)	1 BYTE				
LIMIT CHANNEL FIELD	8 BITS	MAIN CHANNEL FIELD (MMM)	3 BYTES				
CONTROL (LOCAL/REMOTE)	1 BIT	LIMIT CHANNEL FIELD (LL)	2 BYTES				
MODE (VOLTAGE/CURRENT)	1 BIT						
RANGE, MAIN CHANNEL HI/LO	1 BIT						
POLARITY, MAIN CHANNEL +/-	1 BIT						
STROBE	1 BIT	NOTE: SEE SECTION III FOR CODI	NG EXAMPLES				

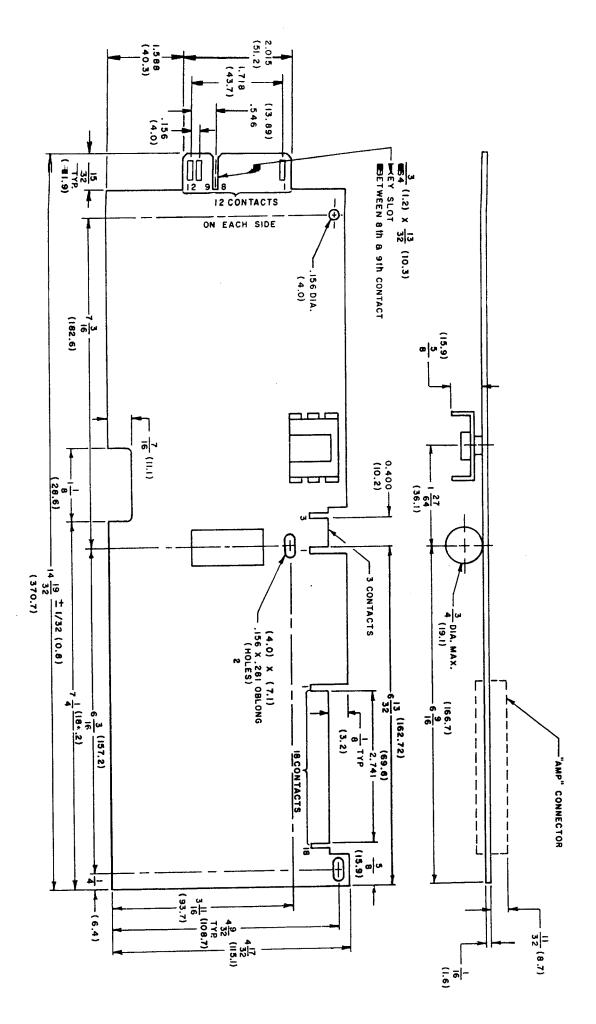
1-12 ACCESSORIES (SUPPLIED)

- A) BIT-BOP INTERCONNECTING CABLE.
- B) DIGITAL INPUT CONNECTOR, KEPCO MODEL PC-12 (BIT-500B and BIT-500D models only).

1-13 ACCESSORIES (OPTIONAL)

A) IEEE-488 (GPIB) BUS INTERCONNECTING CABLES. KEPCO MODEL SNQ 488-1 (1 meter long) or KEPCO MODEL SNQ 488-2 (2 meter long).

(Required for BIT-488B and BIT-488D models only).



SECTION II—INSTALLATION

2-1 UNPACKING AND INSPECTION

2-2 The BIT programming card has been thoroughly inspected and tested prior to packing and is ready for operation following installation. Save original packing material. If any indication of damage is found, file a claim immediately with the responsible transport service.

2-3 INSTALLATION OF BIT CARD INTO THE BOP

STEP 1)

2-4 Installation of the BIT programming card consists of interconnecting the edge connectors of the BIT to the BOP circuitry and securing the card mechanically by means of the provided hardware. Proceed as directed in FIG. 2-1.

INSTALLATION NOTES: Step No's. coincide with encircled No's. on FIG. 2-1.

Remove BOP cover (See Section V, FIG. 5-1

SIEP I)	of your BOP Instruction Manual).
STEP 2)	Remove connector from LOCATION 1 and set aside until Step 5A). This connector has jumper-wires and must be re-installed into LOCATION 1 if the BIT card is removed from the BOP.
STEP 3)	Remove connector from LOCATION 3 and bend aside. 3A) Remove rear CONNECTOR-COVER and discard.
STEP 4)	Unplug ground wire with Q.D. Lug from LOCATION 2. Unpack BIT Card, CONNECTOR HARNESS and knurled mounting nuts. 4A) Connect the ground wire to the Q.D. connector on the BIT card.
STEP 5)	Install BIT card into the GUIDES, slide into position so that mounting holes in BIT card line up with the three (3) mounting posts on the BOP mounting bracket. 5A) Install knurled nuts and lockwashers, securing the BIT card to the mounting posts. Mount the connector, set aside in step 2) into location #4, using the spacer and lockwasher as shown.
STEP 6)	Install the CONNECTOR HARNESS to the BIT card as shown and mate the other side with LOCATION 1.
STEP 7)	Mate the connector, formerly at LOCATION 3, with the BIT card as shown.
STEP 8)	Replace BOP cover. 8A) Affix CONTROL IDENTIFICATION LABEL as shown, its P/N (188-1107) oriented towards the front of the BOP.
STEP 9)	Affix ADDRESS SELECT LABEL (only used with BIT 488-B/D cards) as shown, the number six switch position oriented towards the front of the BOP. The installation of the BIT card is now completed.
STEP 10)	Terminate your BIT card with the provided PC-12 connector (BIT-500) or the optional SNQ-Cable (BIT-488)

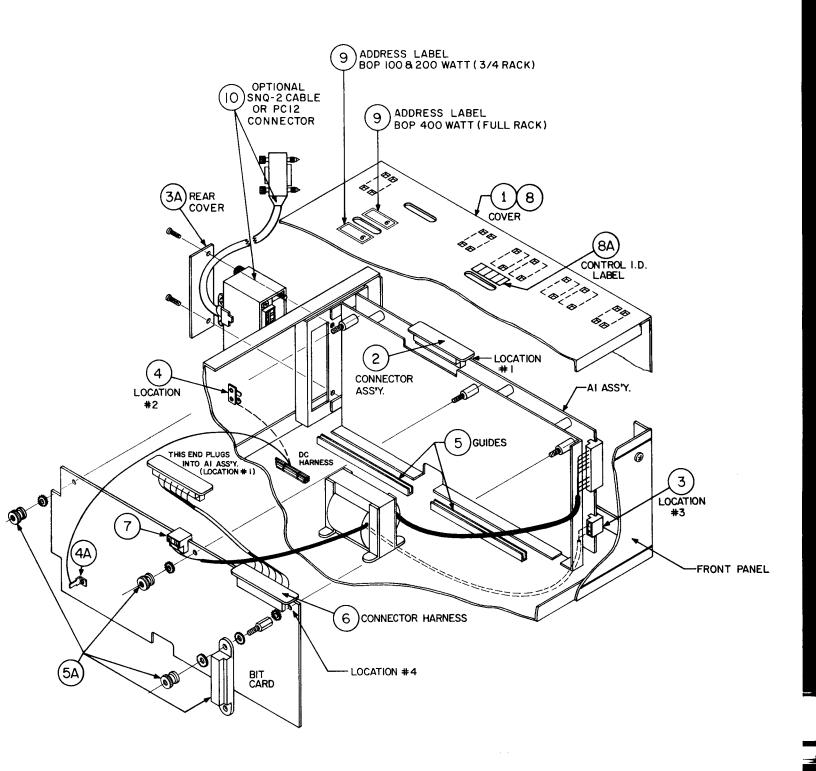


FIG. 2-1 INSTALLATION OF BIT-CARD INTO BOP.

SECTION III-OPERATION

3-1 GENERAL

- 3-2 Operation of the BOP, following the installation of the BIT programming card, requires the following steps:
 - Connect the digital input connector of the BIT card, which is now extending through the rear of the BOP to the data bus.
 - Establish the program to be transmitted via the data bus.

These steps are discussed in detail in the following paragraphs.

- 3-3 Your BOP system, equipped with either a BIT 488 or a BIT 500 digital programming card can be programmed over the full output range of the BOP, bound only by the output specifications given in Section I of the BOP Instruction Manual. Once the BOP is committed to REMOTE CONTROL, either output voltage and output current limit or current and output voltage limit can be controlled simultaneously by means of the BIT-MAIN CHANNEL and LIMIT CHANNEL respectively. Once the MAIN CHANNEL has been committed to voltage or current mode operation, its polarity and resolution can be determined by appropriate bus commands. The LIMIT CHANNEL once dedicated to the control of either the voltage limit (Current Mode Operation) or current limit (Voltage Mode Operation) has a resolution of 8 bits (BIT 488/BIT 500-B Models) or two (2) decades (BIT 488/BIT 500-D Models).
- 3-4 Establishing the program for your digital controlled BOP requires careful study of the digital input signal requirements. These requirements are detailed for both, the BIT 500, as well as the BIT 488 interfaces. Coding examples are presented in paragraph 3-14.

3-5 DIGITAL INPUT DESCRIPTION, BIT 500-B and BIT 500-D.

The Kepco BIT 500 programming cards are designed to receive their input signal via a bit-parallel bus. Either positive or negative logic can be chosen for DATA, POLARITY and RANGE signals by means of a wire jumper on the input connector (PC-12). The RANGE (HI/LO) and the POLARITY (+/-) of the MAIN CHANNEL, as well as the MODE (V/I) and CONTROL (Rem/Loc) functions may be either machine controlled or preselected by hardwiring at the input connector (PC-12). An auxiliary 5V, 20 mA supply is available for special applications.

LOGIC LEVELS: POSITIVE LOGIC: $1 = \text{HIGH} = \ge 2.0 \text{V}, 0 = \text{LOW} = \le 0.8 \text{V}$ NEGATIVE LOGIC: $1 = \text{LOW} = \le 0.8 \text{V}, 0 = \text{HIGH} = \ge 2.0 \text{V}$.

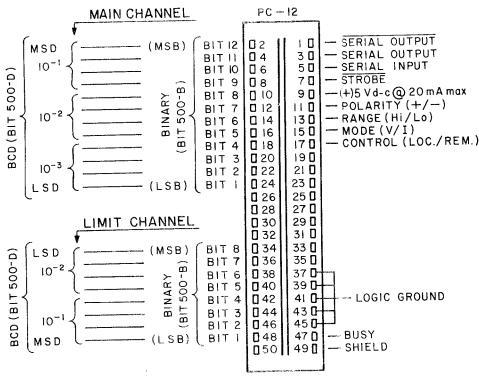


FIG. 3-1 DIGITAL INPUT CONNECTOR WIRING FOR MODEL BIT 500-B AND BIT 500-D NOTE: Unused Pins: 26-32, 19-35, 50

3-5 DIGITAL INPUT DESCRIPTION, BIT 500-B and BIT 500-D (CONT'D)

NOTE: All input commands are with reference to LOGIC GROUND.

A) PIN 5—SERIAL INPUT

WIRE JUMPER FOR

PIN 1—SERIAL OUTPUT

NEGATIVE LOGIC

POSITIVE LOGIC (SUPPLIED)

Pins 1, 3 and 5 serve to select either POSITIVE LOGIC (L=0, H=1) by placing the jumper from pin 5 to pin 3, or NEGATIVE LOGIC (L=1, H=0), by placing the jumper from pin 5 to pin 1. The selection of POSITIVE or NEGATIVE logic applys only to DATA, POLARITY and RANGE signals.

- B) PIN 17—Control (LOC/REM), H = REMOTE, L = LOCAL. Selects either local (FRONT PANEL) or remote (BUS) control of the BOP.
 - NOTE: THIS PIN MUST BE HIGH (H) FOR REMOTE, (BUS) CONTROL OF THE BOP.
- C) PIN 15-MODE (V/I), H = CURRENT Mode, L = VOLTAGE Mode. Determines BOP operating mode.
- Designates the Main Channel to Voltage Control, Limit Channel to Current Limit Control.
- D) PIN 13—RANGE (HI/LO), H = Low Range (0-1V), L = High Range (0-10V). Selects Main Channel output range.
- E) PIN 11—POLARITY (+/-), H = Negative, L = Positive. Selects Main Channel output polarity with reference to ANALOG GROUND.
- F) PIN 9 d-c LOGIC SUPPLY OUTPUT, 5V at 20 mA maximum. May be used to connect pull-up resistors for establishing pre-wired logic states or to drive external logic within the given ratings.
- G) PIN 7—STROBE. The negative going edge signal (H \rightarrow L) enables the loading of the Temporary Storage Registers with the data presented on the <u>data pins</u>. Data must be present for at least 2μ sec. after the negative edge transition (H \rightarrow L) of the <u>STROBE</u> pulse in order to store the data information in the registers.
- H) PIN 47—BUSY (H = busy, L = not busy). This output delivers a status signal to the bus. On the first clock transition (H \rightarrow L), following the STROBE signal, the BUSY line goes high (H) and remains high until the first clock transition (H \rightarrow L), following data transfer (approximately 50 μ sec.), indicating the BIT 500 is ready to accept new data.
- J) PIN 49-SHIELD (CHASSIS). Chassis and Case connection of the BIT 500.
- K) PINS 37, 39, 41, 43, 45 LOGIC GROUND.
- L) MAGNITUDE FIELD, MAIN CHANNEL

PINS:	. 2	.4	6	8	10	12	14	16	18	20	22	24
BITS: (BIT 500-B)	12 MSB	11	10	9	8	7	6	5	4	3	2	1 LSB
DECADE (BIT 500-D)	10-1				10	- 2			10	₁ – 3		
BCD	8	4	2	1	8	4	2	1	8	4	2	1

M) MAGNITUDE FIELD, LIMIT CHANNEL

PINS:	34	36	38	40	42	44	46	48	
BITS: (BIT 500-B)	8 MSB	7	6	5	4	3	2	1 LSB	
DECADE (BIT-500-D)		10	-1		10-2				
BCD	8	4	2	1	8	4	2	1	

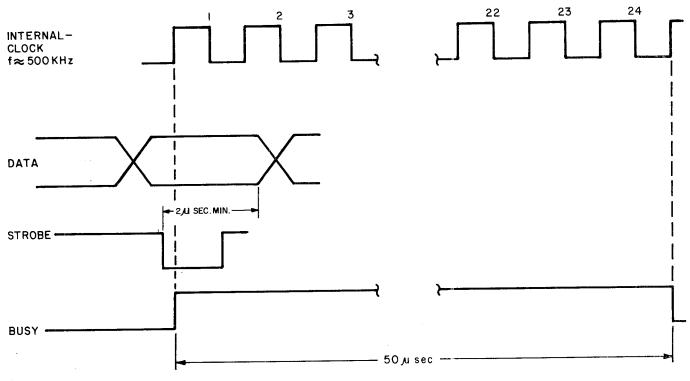


FIG. 3-2 TIMING DIAGRAM, BIT 500 SERIES

3-6 DIGITAL INPUT DESCRIPTION, BIT 488B AND BIT 488D.

- 3-7 The Kepco BIT 488 PROGRAMMING CARDS are designed to receive their input signals via the GPIB (IEEE-488) bus. Once the programming address is manually set as described below (Refer to paragraph 3-8), the BIT 488 card is connected, by means of the digital input cable (Kepco Model SNQ 488-1 or 2) to the GPIB bus. Data rate, input commands, and timing are determined by the GPIB bus protocol and are therefore not described here (See ANSI MC2,1-1975). A general description of the bus is provided in Section IV of this manual.
- 3-8 SETTING THE BIT 488 PROGRAMMING CARD ADDRESS. Locate the Address Selector Switch (S1) on the BIT 488 CARD. Set switch positions according to the selected address (See Table 3-1)

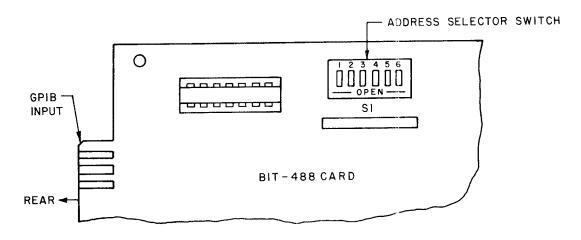


FIG. 3-3 LOCATION OF ADDRESS SELECTOR SWITCH

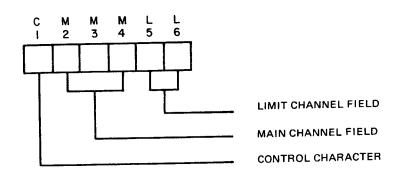
NOTE: The address selector switch (S1) is a miniature multiple rocker switch with positions S1-1 thru S1-6

SWITCH POSITION ON ADDRESS SELECTOR SWITCH (S1)

ASCII CHARACTER	DECIMAL ADDRESS	S1-1	S1-2	S1-3	S1-4	S1-5	LISTEN ONLY S1-6
NOT APP	LICABLE	×	×	×	×	×	0
SP	0	0	0	0	0	0	1
!	1	1	0	0	0	0	1
"	2	0	1	0	0	0	1
#	3	1	1	0	0	. 0	1
\$	4	0	0	1	0	0	1
%	5	1	0	1	o	0	1
&	6	0	1	1	0	0	1
,	7	1 ,	1	1	0	0	1
(8	0	0	0	1	0	1
)	9	1	0	0	1	0	1
*	10	0	1	0	1	0	1
. +	11	1	1	0	1	0	1
,	12	0	0	1	1	0	1 1
-	13	1	0	1	1	0	1
	14	0	1	1	1	0	1
1	15	1	1	1	1	0	1
0	16	0	0	0	0	1	1
1	17	1	0	0	0	1	1
2	18	0	1	0	0	1	1
3	19	1	1	0	0	1	1
4	20	0	0	1	0	1	1
5	21	1	0	1	0	1	1
6	22	0	1	1	0	1	1
7	23	1	1	1	0	1	1
8	24	0	0	0	1	1	1
9	25	1	0	0	1	1	1
:	26	0	1	0	1	1	1
;	27	1	1	ŏ	1	1	1
<	28	0	0	1	1	1	1
=	29	1	0	1	1	1	1
>	30	0	1	1	1	1	1
×	= DON'T CA	ARE		PROGRA	MMING I	NOTE:	
o	= ON (SWITC	CH CLOSE	D)	The comp	olete ASCII	character	(7-bits)
1	= OFF (SWIT	TCH OPEN	l)	must be p	orogramme	ed.	

TABLE 3-1 LISTENING ADDRESS SELECTION ON THE KEPCO BIT 488 SERIES

3-9 INPUT FORMAT, BIT 488 SERIES. Once the address of the BIT 488 Programming Card is set as described in Paragraph 3-8 and the input is connected to the GPIB bus, operation can proceed. Following the LISTENING ADDRESS command, for each program step the BIT 488 card requires the following six byte sequence from the CONTROLLER: (CMMMLL).



- 3-10 Multiple program step instructions may be strung together without a delimiter character. Address and instructions are all ASCII characters. The six program bytes are defined as follows:
- 3-11 BYTE 1; CONTROL CHARACTER BYTE (C): See Table 3-2. The control character byte (C) sets the operating mode of the BOP, determines the BOP output polarity and selects the resolution of the output control. If, for example, the ASCII character "0" is transmitted as the control character byte to a BOP 100-2M with BIT 488-B interface, The BOP is transferred into the voltage mode of operation, the BOP output voltage is controlled by the MAIN CHANNEL FIELD characters (MMM) in the positive output range from 0 to 100 volts with a resolution of 12 bits. If the selected control character is (ASCII) "2" the MAIN CHANNEL FIELD characters (MMM) will now control the BOP output voltage in the range from 0 to 10 volts with a resolution of 12 bits. The selection of the LOW range in the second example is seen to provide 10 times the control resolution over one tenth of the BOP output range.

ASCII CHARACTER	BOP OPERATING MODE	RANGE	POLARITY
0 1 2	VOLTAGE VOLTAGE VOLTAGE	HIGH HIGH LOW LOW	POSITIVE OUTPUT NEGATIVE OUTPUT POSITIVE OUTPUT NEGATIVE OUTPUT
3 4 5 6 7	VOLTAGE CURRENT CURRENT CURRENT CURRENT	HIGH HIGH LOW LOW	POSITIVE OUTPUT NEGATIVE OUTPUT POSITIVE OUTPUT NEGATIVE OUTPUT

TABLE 3-2 CONTROL CHARACTER CODING, BIT 488 MODELS

NOTE: If a digital command string includes a "mode of operation" change (voltage to current or current to voltage mode), transients may occur at the output of the BOP power supply. The transient settling time is approximately 2-3 milliseconds.

A note of caution: If the BOP is operating in the Current Mode, LOW range operation is not recommended, since the high control resolution is swamped out by the output current ripple. A quick calculation shows that in the above example, the resolution in the LOW range would be: $0.2A/4096 \approx 50 \mu A$, while the specified ripple is typically 0.01% of 2A = $0.2mA = 200\mu$ A. While the control character is dedicating the MAIN CHANNEL to either voltage or current mode control, the LIMIT channel is automatically assigned to perform either the complementary voltage or current limiting function. The LIMIT CHAN-NEL resolution is 8 bits (BIT 488-B models) or 2 decades (BIT 488-D models) while the polarity is (fixed) positive. The LIMIT CHANNEL FIELD characters (LL) will determine the output voltage or output current limit value of the BOP.

- 3-12 BYTES 2, 3, 4 (MMM) MAIN CHANNEL FIELD. The magnitude field of the MAIN CHANNEL sets the output voltage or output current of the BOP with a resolution of 12 bits (BIT 488-B models) or 3 decades (BIT 488-D models).
 - A) FOR BIT 488-D models the magnitude field must be three (3) ASCII characters in the range from 0 to 9. The magnitude coding range is therefore from 000 to 999 representing a BOP output quantity (depending on the previous control character of:

```
0 to \pm E_{o max.} (HI RANGE)
```

$$(E_o = BOP output voltage, I_o = BOP output current)$$

- B) FOR BIT 488-B models, the magnitude field must be three (3) ASCII characters in the range from 0 to 9 and A through F (HEX CODE). The magnitude coding range is therefore from 000 to FFF, representing a BOP output quantity (depending on the previous selected control character) of:
 - 0 to ± E_{o max.} (HI RANGE)
 - 0 to $\pm E_{o max}/10$ (LO RANGE)
 - 0 to ± Io max. (HI RANGE)
 - 0 to $\pm I_{o \text{ max.}}/10$ (LO RANGE)

- 3-13 BYTE 5, 6 (LL) LIMIT CHANNEL FIELD. The magnitude field on the LIMIT CHANNEL sets the output voltage limit or output current limit of the BOP with a resolution of 8 bits (BIT 488-B models) or 2 decades (BIT 488-D models).
 - FOR BIT 488-D models the magnitude field must be two (2) ASCII characters in the range from 0 to 9. The magnitude coding range is therefore from 0 to 99, corresponding to a BOP voltage limit (Current Mode Operation) of 0 to $E_{o\ max.}$ (1), or a BOP current limit (Voltage Mode Operation) of 0 to $I_{o\ max.}$ (1), where Eo, Io are the BOP output voltage and current respectively.
 - B) FOR BIT 488-B models, the magnitude field must be two (2) ASCII characters in the range from 0 to 9 and A to F (HEX CODE). The magnitude coding range is therefore from 00 to FF, corresponding to a BOP voltage limit (Current Mode Operation) of 0 to Eo max. (1), or a BOP current limit (Voltage Mode Operational) of 0 to $I_{o\ max.}$ (1), where E_{o} , I_{o} are the BOP output voltage and current respectively.

3-14 CODING EXAMPLES

- 3-15 BIT 500-D MODELS. Example: The output voltage of a BOP 100-2M equipped with a BIT 500-D interface is to be set to 40V, with the current limit at 1.75A. Referring to the BIT 500 input description (Paragraph 3-5) and reviewing the input requirements of our example, we proceed as follows:
 - A) CONTROL LINES
 - 1) Selecting positive logic, pin 5 of the DIGITAL INPUT CONNECTOR (PC-12) is hard-wired to pin 3.
 - Since we want VOLTAGE MODE operation of the BOP, and require a positive output voltage, we select the Hi Range for remote voltage control by the MAIN CHANNEL. Therefore, pins 11, 13 and 15 on PC-12 must be either hardwired to LOGIC GROUND, or a LOW must be transmitted by the CONTROLLER for each program step. Pin 17 must be (HIGH) for remote control.
 - Now, the STROBE (PIN 7) and the BUSY line (PIN 47) are wired to the data bus.
 - The required output levels for each output step can now be coded for the MAIN CHANNEL as shown in Tables 3-3 and 3-5 and for the LIMIT CHANNEL as shown in Tables 3-4 and 3-6.

⁰ to $\pm E_{o \text{ max.}}/10$ (LO RANGE)

⁰ to $\pm I_{o \text{ max.}}/10$ (LO RANGE)

⁽¹⁾ **NOTE:** The quantities $E_{0\ max}$ and $I_{0\ max}$ as applied to the LIMIT CHANNEL are approximely 10% higher than the specified values for each given BOP model. The quantity "zero (0)" as applied to the LIMIT CHANNEL is approximately 0.2% of the specified $E_{0\ max}$ and $I_{0\ max}$ values for each given BOP model.

B) MAIN CHANNEL

1) In our example, all lines except the MAIN CHANNEL bits, stay the same for each program step. The MAIN CHANNEL magnitude bits are coded by referring to Table 3-3 and EQ.3-1.

PC-12 PINS	2	4	6	8	10	12	14	16	18	20	22	24	
DECADE		10	10-1			102				10-3			
	 -	4	2	1	8	4	2	1	8	4	2	1_	
BCD	8	_	0	1	1	0	0	1	1	0	0	1	
FS	1	0	0		0	0	0	0	0	0	0	0	
1/2 FS	0	0	0	0	0	0	0	0	0	0	0	1	
0V + 1 LSB 0 VOLTS	0	ŏ	o	0	0	0	0	0	0	0	0	0	

TABLE 3-3 CODING EXAMPLES, BIT 500D MODELS, MAIN CHANNEL

2) To calculated the BCD coding for any MAIN CHANNEL magnitude the following expression can be used. (BOP in Voltage Model):

$$999/X = E_{o max}/E_{o}$$
 or $X = INTEGER [999 (E_{o}/E_{o max})]$ (EQ.3-1)

Where:

= Full Scale BCD Code

= BCD Code for MAIN CHANNEL magnitude

E_{o max.} = Maximum BOP Output Voltage = Required BOP Output Voltage

3) If, as in the given example, 40 volts output are required from a BOP 100-2M, the BCD code is:

X = INTEGER [999 (40/100)] = 399

C) LIMIT CHANNEL

1) The LIMIT CHANNEL bits are coded by referring to Table 3-4 and EQ.3-2

PC-12 PINS	34	36	38	40	42	44	46	48
DECADE	10-1				10-2			
DECADE		г . ``		1	8	4	2	1
BCD	8	4	2	<u> </u>			<u>├</u>	
FS	1	0	0	1	1	0	0	1
½ FS	0	l 1	lo	1	0	0	0	0
	Ô	0	0	0	0	0	0	1
OV + 1 LSB	ŏ	ľ	0	0	0	0	0	0
O VOLTS	l		<u> </u>					

TABLE 3-4 CODING EXAMPLES, BIT 500D MODELS LIMIT CHANNEL

2) To calculate the BCD coding for any LIMIT CHANNEL magnitude, the following expression can be used (BOP Current Limit):

be used (BOP Current Limit):

$$99/X = I_{o \text{ max}}/I_{o}$$
, or $X = \text{INTEGER} [99 (I_{o}/I_{o \text{ max}})]$ (EQ.2)

Where: 99 = Full Scale BCD CODE

X = BCD CODE, LIMIT CHANNEL MAGNITUDE.

I_{o max.} = Maximum BOP Output Current I_o = Required BOP Output Current

3) If, as in the given example, 1.75A is the required Limit value for a BOP 100-2M, the BCD code is:

X = INTEGER [99 (1.75/2)] = 86

- 3-16 BIT 500-B MODELS (Same Example as in paragraph 3-15)
 - A) CONTROL LINES: Refer to paragraph 3-15A
 - B) MAIN CHANNEL.
 - 1) In our example, all lines, except the MAIN CHANNEL magnitude bits, stay the same for each program step. The MAIN CHANNEL magnitude bits are coded by referring to Table 3-5 and EQ. 3-3.

PC-12 PINS	2	4	6	8	10	12	14	16	18	20	22	24
BITS:	12	11	10	9	8	7	6	5	4	3	2	1
5110.	MSB											LSB
VALUE	2.1	2-2	2.3	2-4	2 -5	2-6	2-7	2.8	2 ⁻⁹	2 ⁻¹⁰	2-11	2-12
FS	1	1	1	1	1	1	1	1	1	1	1	1
³4 FS		1	0	0	0	0	0	0	0	0	0	0
⅓ FS	1	0	0	0	0	0	0	0	0	0	0	0
½ FS	0	1	0	0	0	0	0	0	0	0	0	0
0 VOLTS	0	0	0	0	0	0	0	0	0	0	0	0
1 0 10210	1				l		<u> </u>		<u> </u>	<u> </u>		

TABLE 3-5 CODING EXAMPLES, BIT 500B MODELS, MAIN CHANNEL

 To calculate the binary coding, the following expression can be used: (BOP in Voltage Mode): MAIN CHANNEL magnitude.

(EQ.3-3) FFF/X =
$$E_{o \text{ max}}/E_{o}$$
 or X = INTEGER [FFF ($E_{o}/E_{o \text{ max}}$)]

Where: FFF = Full Scale Binary Code (HEXADECIMAL)

X = Binary Code (HEX) for MAIN CHANNEL magnitude

 $E_{o max.} = Maximum BOP output Voltage$ $E_{o} = Required BOP output Voltage$

3) If, as in the given example, 40 volts are required from a BOP 100-2M, the binary code is: FFF_{16}/X_{16} or: $4095_{10}/X_{10} = 100/40$; therefore: $X_{10} = INTEGER(4095_{10}/2.5) = 1638_{10} = 666_{16}$

C) LIMIT CHANNEL

1) The LIMIT CHANNEL bits are coded by referring to Table 3-6 and EQ. 3-4.

3-8 BIT 488/500-061581A

PC-12 PINS	34	36	38	40	42	44	46	48
BITS	8 MSB	7	6	5	4	3	2	1 LSB
VALUE	2-1	2.2	2-3	2-4	2-5	2-6	2-7	2-8
FQ-1	4	1	1	1	1	1	1	1
¾ FS	1	1	0	0	0	0	0	0
½ FS	1	0	0	0	0	0	0	0
1/4 FS	0	1	0	0	0	0	0	0
0 Volt	0	0	0	0	0	0	0	0

TABLE 3-6 CODING EXAMPLES, BIT 500B MODELS, LIMIT CHANNEL

2) To calculate the binary coding for any LIMIT CHANNEL magnitude, the following expression can be used (BOP current limit):

(EQ. 3-4) FF/X = $I_{o \text{ max}}/I_{o}$, or X = INTEGER [FF ($I_{o}/I_{o \text{ max}}$)].

Where: FF = Full scale binary code (Hexadecimal or base 16)

X = Binary code (Hex.) for LIMIT CHANNEL magnitude

 $I_{o \text{ max.}} = \text{Maximum BOP Output Current}$ $I_{o} = \text{Required BOP Output Current}$

- 3) If, as in the given example, 1.75A are required from a BOP 100-2M, the binary code is: FF_{16}/X_{16} , or $255_{10}/X_{10} = 2/1.75$, or $X_{10} = INTEGER$ [255₁₀ (1.75/2)] = $223_{10} = DF_{16}$
- 3-17 BIT 488-D MODELS: Example: The output voltage of a BOP 50-4M, equipped with a BIT 488-D interface is to be set to 37.5 volts, with the current limit at 3A. Referring to the BIT 488 input description (Paragraph 3-6) and reviewing the requirements of our example, we proceed to code the required command string of 6 ASCII characters (FORM: CMMMLL) as follows:
 - A) CONTROL CHARACTER (Refer to Table 3-1). From the requirements of the example, we select C = 0, i.e. Voltage Mode, Positive Output, High Range.
 - B) MAIN CHANNEL. The three characters needed to code the magnitude of the MAIN CHANNEL (MMM) are selected by referring to Table 3-3 and EQ.3-1. For our specific example:

$$X = INTEGER 999 (37.5/50) = 749$$

C) LIMIT CHANNEL. The two characters needed to code the magnitude of the LIMIT CHANNEL (LL) are selected by referring to Table 3-4 and EQ.3-2. For our specific example.

$$X = INTEGER 99 (3/4) = 74$$

- D) Concatenating the selected "C" value and the two calculated values for the magnitude of the MAIN CHANNEL and LIMIT CHANNEL, the complete command string for our program step is: 074974.
- 3-18 BIT 488-B MODELS (same Example as in paragraph 3-17)
 - A) The control character (Refer to Table 3-1) is from the previous example, C = 0.
 - B) MAIN CHANNEL. The three characters needed to code the magnitude of the MAIN CHANNEL (MMM) are selected by referring to Table 3-5 and EQ.3-3. For our specific example:

$$X = INTEGER [4095_{10} (37.5/50)] = 3071_{10} = BFF_{16}$$

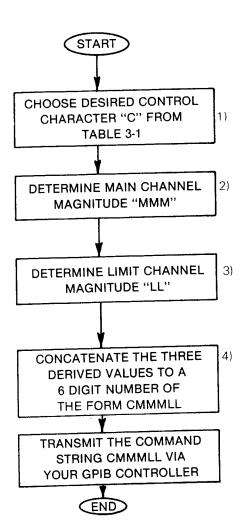
C) LIMIT CHANNEL. The two characters needed to code the magnitude of the LIMIT CHANNEL (LL) are selected by referring to Table 3-6 and EQ.3-4. For our specific example:

$$X = INTEGER [255_{10} (3/4)] = 191_{10} = BF_{16}$$

D) Concatenating the selected control value and the two magnitude values for the MAIN and LIMIT channel, the complete command string for our program step is: 0BFFBF.

3-19 GPIB PROGRAMMING NOTES FOR THE EXPERIENCED USER

- 1) The BOP, equipped with a BIT 488 interface, functions as a LISTENER on the GPIB bus, similar to a printer. In fact, any command or series of commands needed by your GPIB CONTROLLER to output data to a printer, will function equally well for producing the selected output from your BOP-BIT 488 system.
- 2) Users familiar with the GPIB bus will therefore quickly realize that the 6 byte command string for the BOP-BIT 488 systems is to be placed between the MLA and the UNL commands as issued by the GPIB CONTROLLER.
- 3) We strongly recommend that the user familiarize himself with the way his particular controller implements the GPIB interface. There are, for example, subtle differences in the way the PET and the TEKTRONIX 4051 desk computers handle the REN (local/remote) line. Whereas the PET ties this line simply to logic ground, on the TEKTRONIX 4051 it is an active line and will return to HIGH automatically after completion of the program. In practical terms this means, since the BOP-BIT 488 systems does not have LOCAL/REMOTE front panel control, it can only return to LOCAL control (with the PET controller) if the controller is either physically disconnected from the bus or if a machine program is written to implement GTL (go to LOCAL) after completion of a program.
- 4) GENERAL PROCEDURE TO FORM THE 6-BYTE COMMAND STEP FOR YOUR BOP-BIT 488 SYSTEM.



FLOW-CHART COMMENTS:

Note: Coding Example based on BOP 100-2M-488D.

- Determine the required operating conditions for your application. Select the control character from Table 3-1. Example: Voltage Mode, High Range, Negative Output, C = 1
- Using the given equation (EQ.3-1) calculate the required magnitude field for the MAIN CHANNEL. Example: For an output voltage of 30 volts the BCD value is 299. Therefore MMM = 299.
- 3) Using the given equation (EQ.3-4) calculate the required magnitude field for the LIMIT CHANNEL. Example: For a current limit of 1.75A the BCD value is 86. Since two digits must be programmed, LL = 86
- 4) Concatenating the selected "C" value and the two calculated values, the complete commands for our program step is: CMMMLL = 129986

BIT 488/500-061581A

3-20 SYSTEM CALIBRATION

- 3-21 EQUIPMENT REQUIRED:
 - BOP with BIT card installed
 - SYSTEM CONTROLLER
 - 3) DG DIGITAL YOLTMETER, 0-100 volts (M1), at least 1 mV resolution.
- 3-22 The BOP/BIT digitally programmable bipolar power supply is factory calibrated to perform Within the specifications outlined in Section 1 of this manual. For the purpose of recalibration and for the case where the BIT card is installed by the user, the calibration procedure is described below.

WARNING

STANDARD HIGH VOLTAGE PRECAUTIONS MUST BE TAKEN IF THE ANALOG OUTPUT OF THE BOP/BIT IS NOT GROUNDED (FLOATING). USE INSULATED SCREWDRIVERS AND TEST PROBES FOR ALL ADJUSTMENTS.

- 3-23 ACCURACY. The BOP/BIT power supply will respond to the programmed digital input with the accuracy specified in Section I of this manual if the calibration procedure is performed as described.
- 3-24 RESOLUTION. Since the BOP/BIT power supply is capable of resolving voltage and current steps within the magnitude of its specified output ripple and noise, any external connections made to the device must be made with the utmost care. Please refer to your BOP instruction manual for load connection and grounding information.
- 3-25 BOP OUTPUT ZEROING. Before proceeding to calibrate the BOP/BIT system, the BOP should be checked for zero output with zero signal input. Either test set-up in FIG. 3-5 can be used, depending on whether the BOP is used in the voltage mode (Front panel MODE switch in the VOLTAGE position), or in the current mode (Front panel MODE switch in the CURRENT position).
 - Set the BOP front panel VOLTAGE CONTROL switch (or the CURRENT CONTROL switch if operating in the current mode) to the OFF position.
 - Turn the BOP POWER switch to the ON position. Observe the BOP front panel REMOTE light, it should be off (BOP in local control mode). If the BOP output is not zero, adjust the appropriate calibration control (See FIG. 3-4 for location).

3-26 SYSTEM CALIBRATION, PROCEDURE

NOTE: For optimum accuracy, allow a one hour warm-up time for the complete calibration set-up. Refer to FIG. 3-4 for the location of all controls needed in this procedure. Refer to the applicable test set-up BOP CONT. CARD drawing in FIG. 3-5.

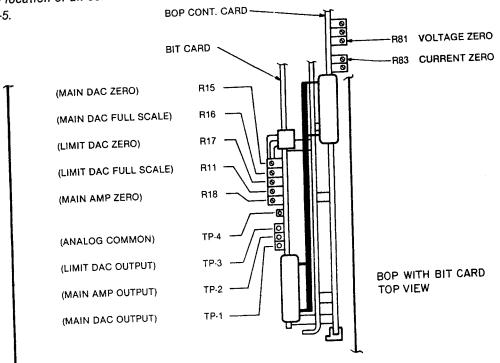
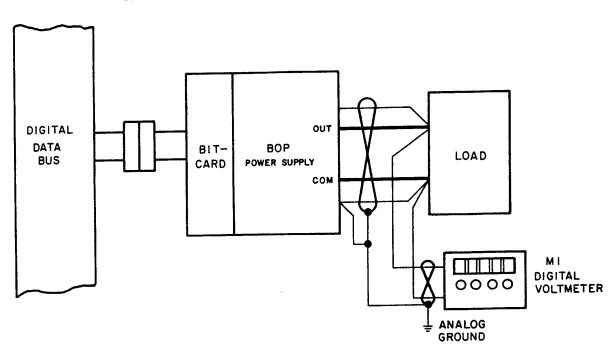


FIG. 3-4 LOCATION OF CALIBRATION CONTROLS AND TEST-POINTS, BOP WITH BIT-CARD.

3-27 Proceed with the calibration as directed on the FLOW CHART, FIG'S. 3-5 and 3-6. The chart instructions are directly applicable for the BOP/BIT system operating in VOLTAGE mode. With the system operating in CURRENT mode, (+)M1 is connected to "(+)R_M" instead of "BOP output", see FIG. 3-5. All other steps are the same. R_M is a 4 terminal measuring resistor, selected to drop one (1) volt at the maximum operating current of the BOP.

CALIBRATION SET-UP FOR BOP VOLTAGE MODE OPERATION.



CALIBRATION SET-UP FOR BOP CURRENT MODE OPERATION.

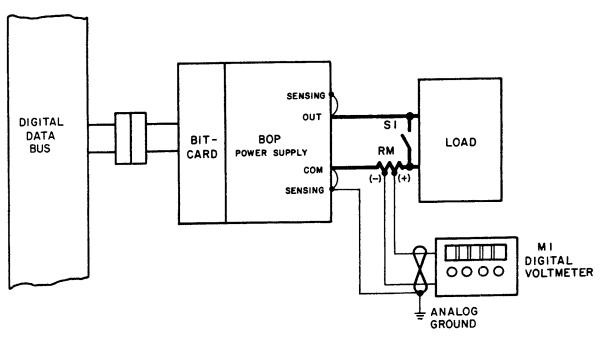
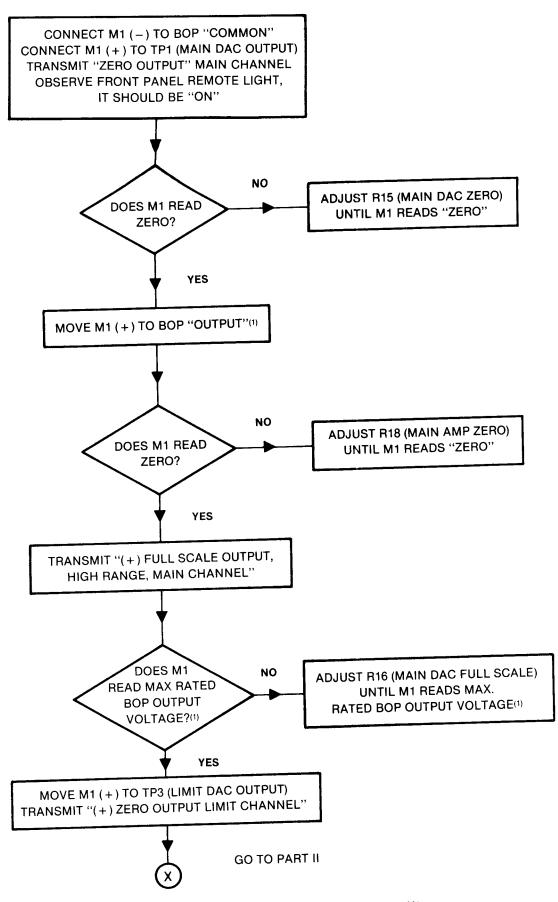


FIG. 3-5 TEST SET-UPS FOR CALIBRATION OF THE BOP/BIT SYSTEM



(1) With the BOP/BIT System operating in the current mode, connect (+)M1 to (+) $R_{M},$ see FIG. 3-5. Calibrate to 1.00 volts at maximum output current.

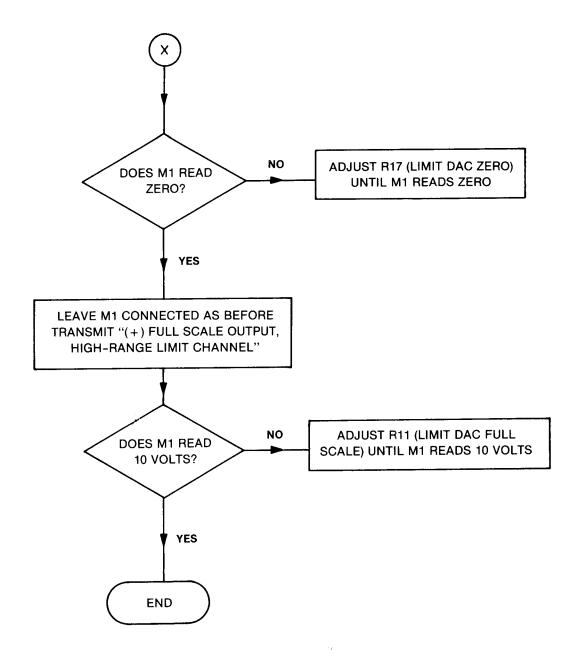


FIG. 3-7 CALIBRATION FLOW-CHART, PART II

- NOTES: 1) The calibration as described in the previous paragraphs, is valid for either the voltage mode or the current mode of operation, not both.
 - In any given application, therefore, it is necessary to designate the operating mode which requires precision output and calibrate in this mode. If the complementary operating mode is required, the calibrating procedure must be repeated for this mode.
 - 2) If a digital command string includes a "mode of operation" change (voltage to current or current to voltage mode), transients may occur at the output of the BOP power supply. The transient settling time is approximately 2-3 milliseconds.